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Design of 8-Bit Processor Element using Adiabatic Reversible Logic

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Abstract:
Low power design has become one of the primaries focuses in portable/embedded devices, where energy supplies are limited. To achieve low power consumption reversible logic becomes a competent technology where power dissipation becomes a limiting factor on performance. In modern VLSI (Very Large-Scale Integration), system power dissipation is very high due to rapid switching of internal signals. The complexity of VLSI circuits increases with miniaturization of integrated circuits every year due to packing more and more logic elements into smaller volumes. The reduction of power dissipation has become a crucial issue in today's hardware design process. The foremost aim of this research is to develop a novel 8-bit processing element which supports 8-bit addition, subtraction and multiplication using a new 3-vector input and 3-vector output reversible gate named Modified Toffoli using Gate Diffusion Input technique (MTGDI). The power reduction in the processing element can be achieved by using adiabatic reversible logic. The logic technique deployed in developing this 3-to-3 reversible logic gate is Gate Diffusion Input Technique (GDI). The versatile features of this proposed gate produce optimum number of garbage outputs and quantum cost with compared to the existing counterpart. To achieve this aim two objectives have been fixed. The former goal defines the creation of 3-to-3 reversible logic gate using synthesizable GDI library and the latter goal defines the creation of results of MTGDI gates in terms of rise time, fall time and total delay will be fully furnished. The propagation delay is observed, and the average of propagation delay of the inputs has been reported as the total delay of the circuit. The power consumption has been measured for all the bit combinations and its average power has been reported as follows: The proposed design has achieved magnificent results in regards to the design 8-bit processor.

Keywords: Reversible computing, 8-Bit Processor, adiabatic logic

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1. Introduction

In modern VLSI system power dissipation is very high due to rapid switching of internal signals. The complexity of VLSI circuits increases with miniaturization of integrated circuits every year due to packing more and more logic elements into smaller volumes. Hence power dissipation has become the main area of concern in VLSI design. The reduction of power dissipation has become a crucial issue in today's hardware design process. Traditional irreversible circuits generate heat due to the loss of information during computation.

According to scientist R. Land Auer's research in 1961, the amount of energy dissipated for every irreversible bit operation in a system T is the temperature at which operation is performed [1]. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components. In 1973, Bennett showed that kTln (2) energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs [2]. He inferred that amount of energy dissipation would not occur if a computation is carried out in a reversible way using reversible logic.

Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs Energy dissipation can be reduced or even eliminated if computation becomes Information lossless. Thus, reversible logic appears to be promising in future low power design applications [3].

1. Classification of Bit Ripple Carry Adder Design

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and the inputs can be uniquely recovered from the outputs. Also, in the synthesis of reversible circuits direct fan-out is not allowed as one to many concepts is not reversible [4]. However, fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

The reversible circuit/gate has the following characteristics [5]:

(i) Has equal number of inputs and outputs
(ii) The gate output which is not used as primary output in the circuit is called garbage output
(iii) The input which is used as control input to the gates is called constant/garbage input
(iv) The fan-out of each gate is equal to one. A copying circuit is used if two copies of a signal are required

An efficient design in reversible logic should have the following features [5]:

(i) Minimum number of reversible logic gates
(ii) Should have less number of garbage outputs
(iii) Less number of constant inputs and
(iv) Minimization of quantum cost

2.1 Basic Reversible Logic Gates

Feynman Gate*:* Feynman gate [5] is a 2*2 reversible gate as shown in Figure 1. The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P=A, Q=A ⊕B. Quantum cost of a Feynman gate is 1. Feynman gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs. Feynman gate is also known as Controlled NOT (CNOT) gate.

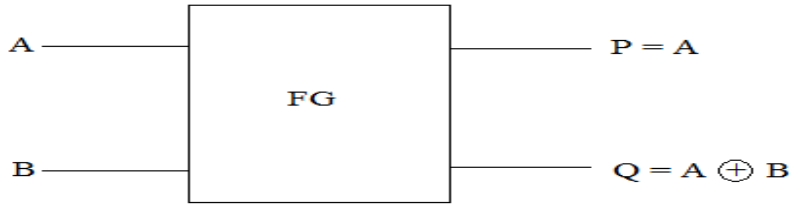

Figure 1. Feynman Gate [5]

Toffoli Gate*:* Figure 2 shows the 3*3 Toffoli gate (TG) [5]. The input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB⊕C. Toffoli gate is one of the most popular gate. Quantum cost of a Toffoli gate is 5.

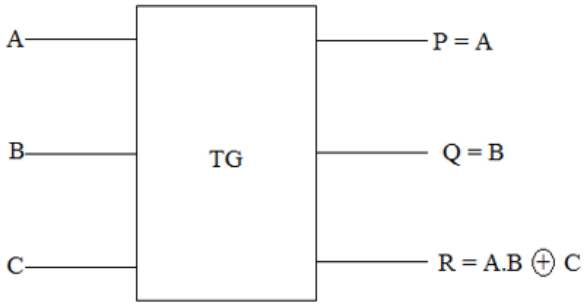

Figure 2. Toffoli Gate [5]

Fredkin Gate: Three input and three output (3*3) reversible Fredkin gate [5] shown in Figure 3. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B⊕AC and R=A′C ⊕ AB. Quantum cost of a Fredkin gate is 5.

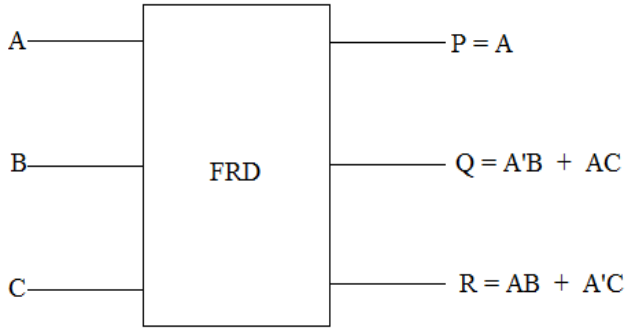

Figure 3. Fredkin Gate [5]

Peres Gate: Peres gate [6] having 3 inputs and 3 outputs(3*3) reversible gate shown in Figure 4. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A⊕B and R=AB ⊕ C. Quantum cost of a Peres gate is 4. Peres gate has the minimum number of quantum cost.

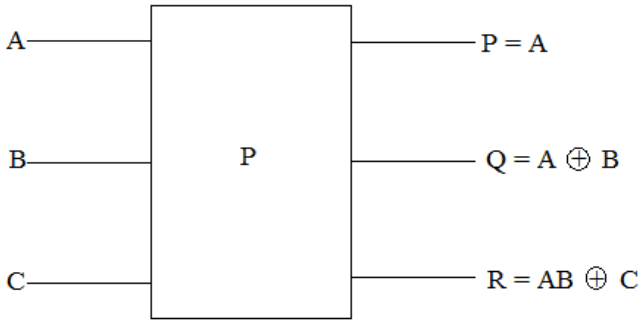

Figure 4. Peres Gate [6]

TSG Gate: Reversible 4*4 TSG gate [7] block diagram shown in Figure 5. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S).

The output is defined by P = A, Q = A'C'⊕B',R = (A'C'⊕B') ⊕ D and S =(A'C'⊕B').D⊕ (AB⊕ C). Quantum cost of a Peres gate is 4.

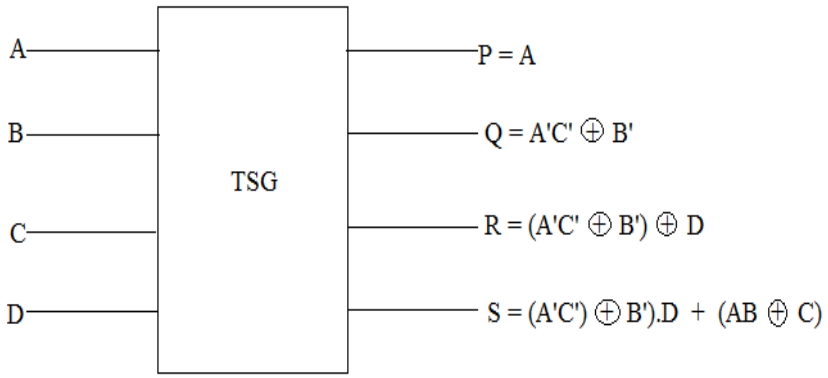

Figure 5. TSG Gate [7]

SayemGate: Sayen gate [5] is a 4 inputs and 4 outputs reversible gate. The input and output vector of this gate are I = (A, B, C, D) and O = (A, A'B ⊕AC, A'B ⊕ AC⊕ D, AB ⊕ A'C ⊕D).The block diagram of this gate is shown in Figure 6

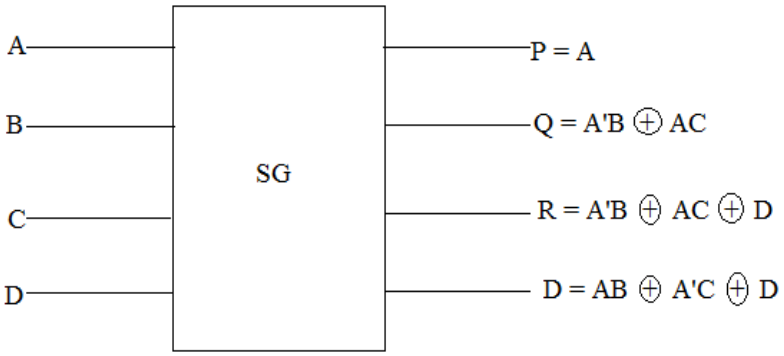

Figure 6. Sayem Gate [5]

TR Gate: The reversible TR gate [8] is a 3 inputs 3 outputs(3*3) gate having inputs to outputs mapping as (P=A, Q=A⊕B, R = A B' ⊕ C) as shown in Figure 7, where A,B,C are inputs and P,Q,R are the outputs respectively.

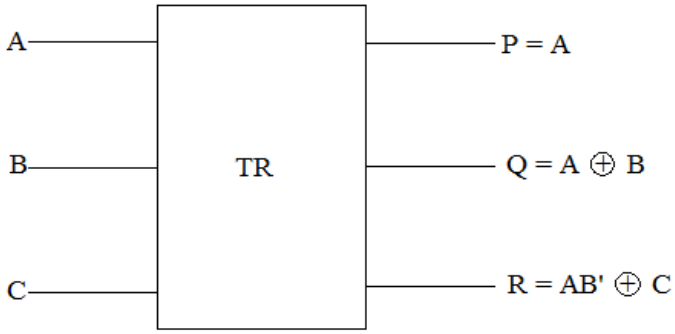

Figure 7. TR Gate [8]

DKG Gate: DKG gate [9] is a 4*4 reversibl logic gate. DKG gate with inputs A, B, C, D and outputs are P, Q, R, S. the DKG gate with 4*4 inputs and outputs shown Figure 8.

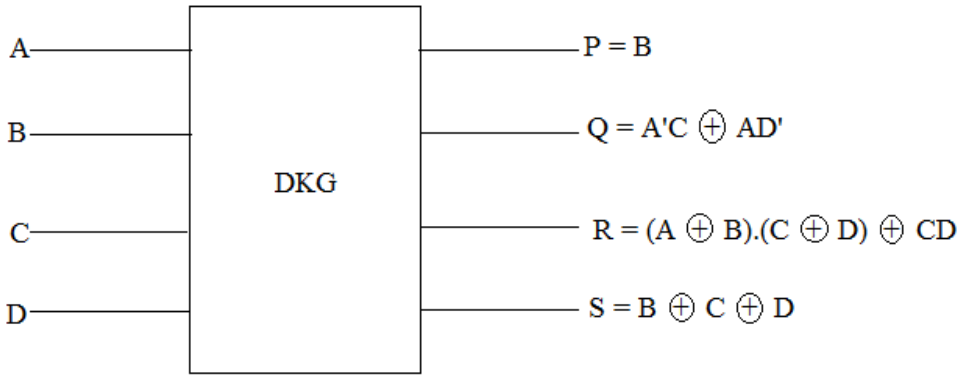

Figure 8. DKG Gate

2.2 Carry Look Ahead Adder Design

The full adder is the basic building block in the ripple carry adder [10]. The full adder circuit using the TSG gate is shown in Figure 9. The ripple carry adder is obtained by cascading the full adders in series as shown in Figure 9. The output expressions for a ripple carry adder are:

$$S_i = X \oplus Y \oplus C_i$$

$$C_i = (X \oplus Y).C_i \oplus XY \quad (i = 0, 1, 2 \ldots\ldots)$$

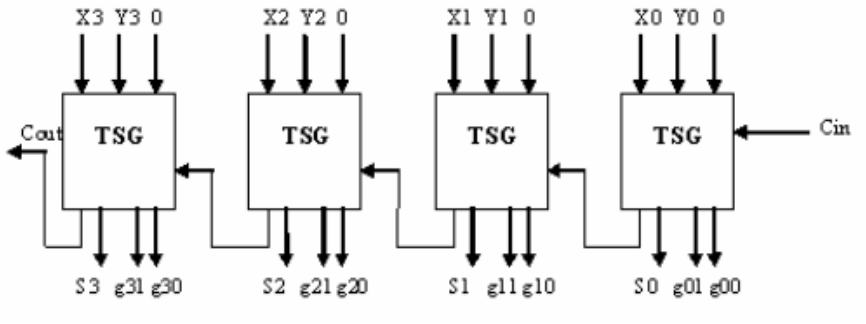

Figure 9. Ripple Carry Adder Using TSG Full Adder [10]

This ripple carry adder architecture uses only N reversible gates and produces only 2N garbage output. The layout of a ripple-carry adder is simple, which allows for fast design time. However, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder.

Table 1. Trust table of Feynman Gate

Input		Output	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

2. Methodology

The main theme of this paper is to implement the reversible arithmetic circuit blocks using gate diffusion input (GDI) logic design technique. Initially all the existing reversible logic gates are converted into GDI based circuit and Arithmetic units such as full adder, carry look ahead adder,

This study explores the effect of the design of the base reversible logic circuit in the overall design and explores methods to reduce power dissipation using reversible design with gate diffusion input technique. Figure 10 shows the flowchart of design procedure for reversible, which is started by background study of the various articles with proper planning literature review of the topic is to the topic is to be done followed by the selection of methodology to meet the objectives. For design reversible logic mentor graphics software is to be used with pyxis design manager to perform simulation when the requirements are matched implementation of the design is done, if not then the design parameters are changed.

Design steps

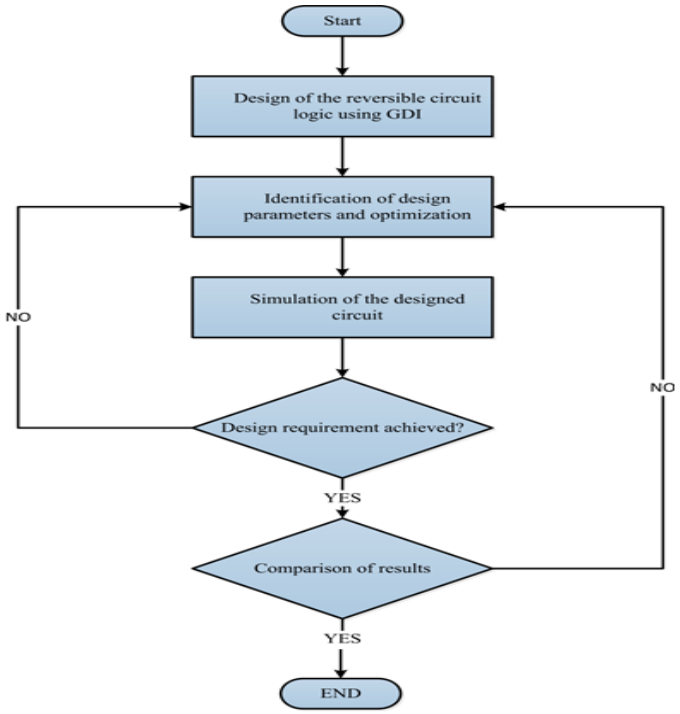

Figure 10. Flowchart of Reversible Circuit Design Procedure

3. Results and discussion

Reversible logic design is extensively motivated in recent years due to its energy and information lossless design. Conventional irreversible logic gates dissipate heat for every single bit loss during their operation. Based on Rylander's theory in 1960, the loss of one-bit information dissipates kTln(2) joules of energy. is the Boltzmann's constant and T is absolute temperature at which operation is occurred [1]. This loss cannot be avoided if the circuit comprises of irreversible logic gates. In 1973, Bennet demonstrated that this kTln (2) joules dissipation can be avoided if the circuit is reversible [2]. So, this power dissipation issue can be overcome by using reversible logic gates instead of conventional irreversible logic gates in a circuit.

The incentive for using reversible computation models comes from the prospect of removing the energy dissipation that is caused by information destruction. This is due to the characteristics of forward and backward deterministic of reversible logic. A gate or circuit is reversible if it does not lose any information and allows one to uniquely recover input vector from the output vector and vice versa. In reversible logic gates, there is one to one mapping between input and output i.e. number of input lines equal to number of output lines. This objective mapping prevents the loss of information which is main reason for power dissipation in irreversible logic. The reversible gate output which is not used is called Garbage output. Extra Inputs which are used in reversible gate to make it reversible is called Constant or Garbage input.

Performance and Complexity of reversible gate/circuits depends on various parameters. Such as

- Less number of reversible logic gates are used to design reversible circuit
- Less number of constant or garbage input should be used to make the gate reversible
- Garbage output should be minimum
- Fan out is not allowed in reversible logic gate. The fan out for each gate is equal to one. A copying gate is used if more fan out is required.

Proposed Reversible Logic Gates:

MTGDI1 Gate

MTGDI gate1 is a 3*3 reversible gate as shown in Figure 11. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P=A, Q = AB+A'C, R = B ⊕ AC.

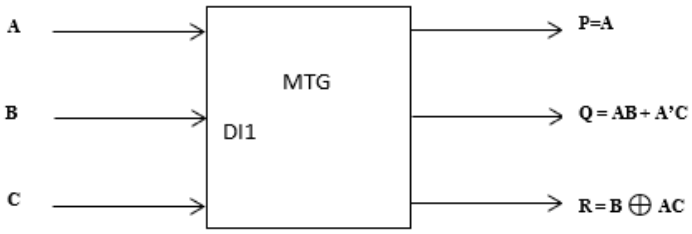

Figure 11. MTGDI1 Gate

MTGDI2 Gate

Figure 12 shows a 3*3 MTGDI gate2. The input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P = A', Q = A ⊕ B ⊕ C, R = C'

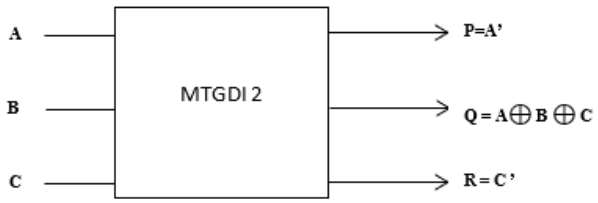

Figure 12. MTGDI2 Gate

MTGDI3 Gate

MTGDI GATE3 is 3x3 reversible gate. The input and output vector of this gate are, I = (A, B, C) and O = (B, A, A'B' ⊕ C). The block diagram of this gate is shown in Figure 13

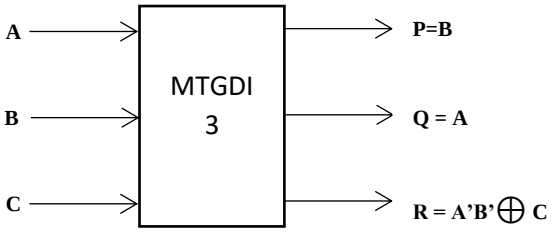

Figure 13. MTGDI3 Gate

MTGDI4 Gate

The reversible MTGDI GATE4 is a 3 inputs 3 outputs gate having inputs to outputs mapping as (P = A, Q = A⊕B⊕C, R = C as shown in Figure 14

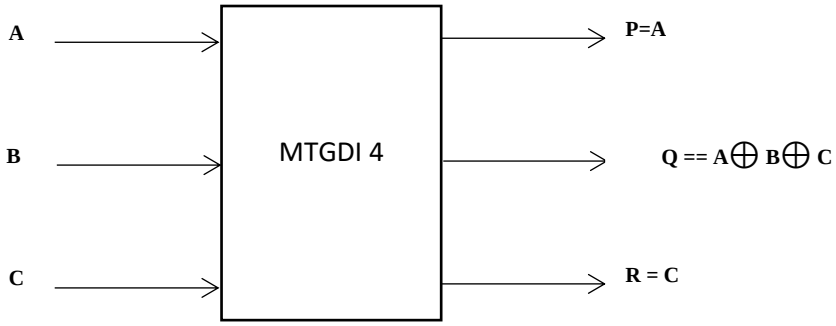

Figure 14. MTGDI4 Gate

MTGDI GATE5 is 3*3 reversibl gate. MTGDI5 Gate gate with inputs A, B, C and outputs are P = A, Q =A⊕B and R =A⊕B⊕C shown in the Figure 15.

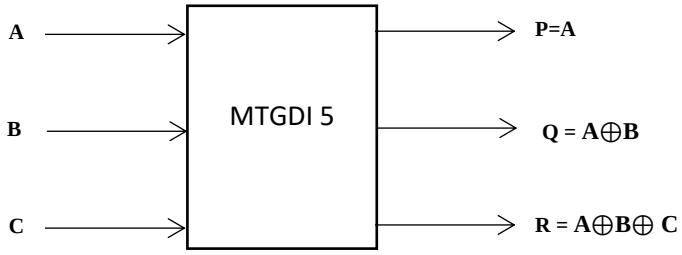

Figure 11. MTGDI5 Gate

MTGDI6 Gate

Figure 16 shows a 3*3 MTGDI6 is defined by P = A, Q = A⊕B and R= C. Gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output

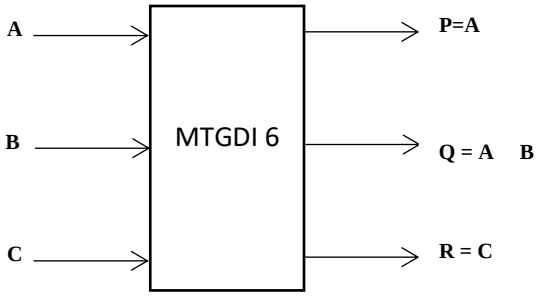

Figure 12. MTGDI6 Gate

4. Comparative Analysis of MTGDI gates

In comparison of different logic, the superiority of the design not only depends on power, delay and transistor count but also on PDP (Product of power and delay) and AT (Product of transistor count (area) and delay) values. The comparisons of PWR (Power), PDP and AT are presented in Table 2. The percentage improvement in power, PDP and AT for various logic with respect to proposed logic is shown in Table 3.

Table 2: Delay of MTGDI gates for different logic design techniques.

Logic	Proposed Gate	Delay1 (ns)				Delay2 (ns)				Delay3 (ns)				Total Delay(ns)
		A to P	A to Q	A to R	Avg	B to P	B to Q	B to R	Avg	C to P	C to Q	C to R	Avg	
GDI	Gate1	0.041	44.8	29.83	24.89	30.04	14.8	0.16	15	45.04	0.196	15.16	20.13	20
	Gate2	0.011	44.97	44.93	29.97	30.01	14.97	14.93	19.97	45.01	0.02	0.064	15.03	21.65
	Gate3	29.88	0.105	39.91	23.29	0.117	30.1	9.91	13.37	15.11	45.1	5.089	21.76	19.48
	Gate4	0.082	44.95	44.87	29.96	30.08	14.95	14.87	19.96	45.08	0.047	0.124	15.08	21.67
	Gate5	0.042	19.88	44.8	21.57	30.04	10.11	14.8	18.31	45.04	25.11	0.194	23.44	21.11
	Gate6	0.136	30.02	44.87	25.01	30.13	0.023	14.87	15	45.13	14.97	0.125	20.07	20.03
CMOS	Gate1[17]	0.165	44.72	29.78	24.88	30.16	14.72	0.218	15.03	45.16	0.272	15.21	20.21	20.04
	Gate2	0.058	39.78	44.94	28.25	30.05	9.782	14.94	18.25	45.05	5.217	0.052	16.77	21.09
	Gate3	29.84	0.129	44.76	24.9	0.156	30.12	14.76	15.01	15.15	45.12	0.23	20.16	20.02
	Gate4	0.16	39.78	44.83	28.25	30.16	9.784	14.83	18.25	45.16	5.215	0.163	16.84	21.12
	Gate5	0.153	19.84	44.78	21.59	30.15	10.15	14.78	18.36	45.15	25.15	0.214	23.5	21.15
	Gate6	0.16	19.78	44.84	21.59	30.16	10.22	14.84	18.4	45.16	25.22	0.152	23.51	21.17
TG	Gate1	0.161	44.77	29.93	24.95	30.16	14.77	0.06	14.99	45.16	0.221	15.06	20.14	20.03
	Gate2	0.059	44.91	44.94	29.96	30.05	14.91	14.94	19.96	45.05	0.085	0.06	15.06	21.66
	Gate3	29.84	0.135	40.01	23.32	0.151	30.13	10.01	13.43	15.15	45.13	4.983	21.75	19.5
	Gate4	0.152	44.91	44.83	29.96	30.15	14.91	14.83	19.96	45.15	0.085	0.167	15.13	21.68
	Gate5	0.161	30.03	44.86	25.01	30.16	0.037	14.86	15.01	45.16	14.96	0.133	20.08	20.04
	Gate6	0.152	30.08	44.84	25.02	30.15	0.08	14.84	15.02	45.15	14.91	0.153	20.07	20.03

Table 3: Power dissipation of MTGDI gates for different logic design techniques

Logic	Proposed Gate	PWR (W) A(V1)	PDP (µW× ns in fW-s)	Rise Time (ns)			Fall Time (ns)			# Tr	AT(#Trns)
				P	Q	R	P	Q	R		
GDI	Gate1[15]	873.60µ	17479.38	0.249	0.076	0.257	0.217	0.103	0.104	24	480.2
	Gate2	802.24µ	17374.82	0.287	0.298	0.235	0.288	0.048	0.435	16	346.52
	Gate3	693.00µ	13499.79	0.09	0.095	0.072	0.087	0.235	0.053	22	428.56
	Gate4	788.14µ	17081.53	0.09	0.07	0.079	0.208	0.241	0.082	20	433.46
	Gate5	830.79µ	17540.93	0.248	0.085	0.074	0.217	0.082	0.103	26	548.95
	Gate6	784.36µ	15711.52	0.07	0.243	0.088	0.409	0.048	0.082	16	320.49
CMOS	Gate1[17]	1.44m	28864.8	0.113	0.071	0.162	0.102	0.061	0.171	43	861.93
	Gate2	1.01m	21307.51	0.306	0.171	0.314	0.605	10.14	0.337	30	632.89
	Gate3	1.11m	22232.69	0.122	0.178	10.08	0.162	0.232	0.083	31	620.91
	Gate4	1.07m	22598.64	0.121	0.16	0.131	0.103	10.14	0.111	34	718.08
	Gate5	1.19m	25170.75	0.235	0.244	0.179	0.104	0.527	0.174	34	719.16
	Gate6	1.07m	22652.14	0.121	0.16	0.235	0.104	0.061	0.111	21	444.57
TG	Gate1[24]	12.93m	259019.5	0.104	0.203	0.284	0.116	0.138	0.512	46	921.49
	Gate2	4.12m	89268.51	0.592	0.293	0.304	0.493	10.11	0.3	20	433.34
	Gate3	955.34 µ	18633.27	0.124	0.182	10.01	0.18	0.115	0.353	28	546.12
	Gate4	4.14m	89784.64	0.126	0.291	0.167	0.119	10.11	0.102	24	520.49
	Gate5	14.91m	298798	0.105	20.47	0.291	0.118	0.324	0.4	28	561.12
	Gate6	4.27m	85568.42	0.128	0.231	0.235	0.119	0.475	0.103	16	320.63

P	Gate1[25]	1.32m	26424.93	0.235	0.047	0.084	0.114	0.036	0.213	48	960.9
T	Gate2	3.80m	80218.42	0.553	0.083	0.302	0.299	0.131	0.3	24	506.64
	Gate3	1.12m	21840.87	0.124	0.121	0.088	0.118	0.115	0.07	30	585.02
	Gate4	3.98m	84113.32	0.103	0.077	0.107	0.119	0.056	0.103	28	591.75
	Gate5	1.23m	26002.61	0.107	0.088	0.084	0.119	0.045	0.037	32	676.49
	Gate6	3.99m	80019.45	0.102	0.072	0.235	0.119	0.044	0.104	18	360.99
C	Gate1[16]	1.55m	31054.94	0.103	0.056	0.164	0.232	0.053	0.295	51	1021.8
P	Gate2	3.97m	83862.73	0.585	0.156	0.31	0.302	10.26	0.297	22	464.73
L	Gate3	1.06m	20893.31	0.124	0.117	0.06	0.115	0.114	0.19	30	591.32
	Gate4	4.05m	85623.29	0.105	0.154	0.12	0.119	10.26	0.103	26	549.68
	Gate5	4.39m	88045.36	0.102	19.86	0.123	0.119	0.181	0.08	31	621.73
	Gate6	4.11m	86914.64	0.105	0.138	0.235	0.119	20.46	0.104	17	359.5
D	Gate1[17]	13.64m	273206.2	0.103	0.25	0.62	0.114	0.182	0.595	46	921.36
PL	Gate2	3.62m	78573.29	0.592	0.621	0.303	0.304	0.27	0.301	20	434.1
	Gate3	1.07m	20878.32	0.235	0.118	10.29	0.115	0.115	0.573	28	546.34
	Gate4	3.63m	78861.35	0.163	0.62	0.112	0.119	0.271	0.102	24	521.39
	Gate5	6.90m	145942.7	0.103	20.81	0.621	0.118	0.344	0.602	28	592.23
	Gate6	3.28m	65755.97	0.107	0.652	0.235	0.119	0.335	0.123	16	320.76

The first MTGDI6 gate produces $M \oplus B$ and the second MTGDI6 and MTGDI1 produce the full adder operation. The EX-OR block is implemented with MTGDI6 which receives three inputs namely M,B and C and produces three outputs P=M, Q=M⊕B and R=c. When the input M=0 the Q output produces true (uncomplemented) value of B. The other two outputs act as buffer. In this case it is garbage output. The Q output from first module is given to full adder circuit. The full adder module is constructed using 2-MTGDI6 gates and 1-MTGDI1 gate. The upper part of MTGDI6 gate receives three inputs namely A, Q and M and consequently gives three outputs P=A, Q1=A^Q and R=C. Here also only Q1 output is used and the remaining two outputs are garbage. The lower part of MTGDI6 gate receives three inputs namely cin, Q1 and C and consequently gives three outputs P=cin, Q2=A⊕Q1 and R=C. Here also only Q1 output is used and the remaining two outputs are garbage. The output of Q1 and inputs cin and A are given to MTGD1 gate for producing the carry out signal (cout).

In the transistor representation only the inputs, sum and count outputs are shown. The garbage outputs P and R are not represented in the circuit diagram. Totally there are 8 unused outputs per cell, therefore 8*8=64 garbage outputs are present in the entire 8-bit adder/subtractor module. It is one of the deficits in this circuit; on the other hand, delay and power aspects are optimal. The 8-bit computation process for M=0 and M=1 are also demonstrated in the preceding sections. The total number of transistors required to implement this adder/subtractor module is 80 which excludes the level restoration circuit.

6. Simulation Results of Proposed MTGDI Gates

The simulation results of various reversible circuits obtained using mentor graphics pyxis are discussed. All the schematics are based on TSMC 130nm technology with supply voltage ranging from 1.2V to 5V in steps of 0.2V. All the circuits are simulated with multiple design corners to verify that operation across variations in device characteristics and environment. The W/L ratios of both nMOS and pMOS transistors are taken as 2.5/0.25µm. The circuits are simulated with a 100MHz clock frequency. The delay parameter is calculated from all the transitions from an input combination to another, and the delay at each transition has been measured from the time that clock signal reaches 50% of the supply level. Power delay product (PDP) has been calculated by the taking the product term of delay and average power consumption. The input/output waveform generated for proposed full adder with clock frequency of 100MHz.

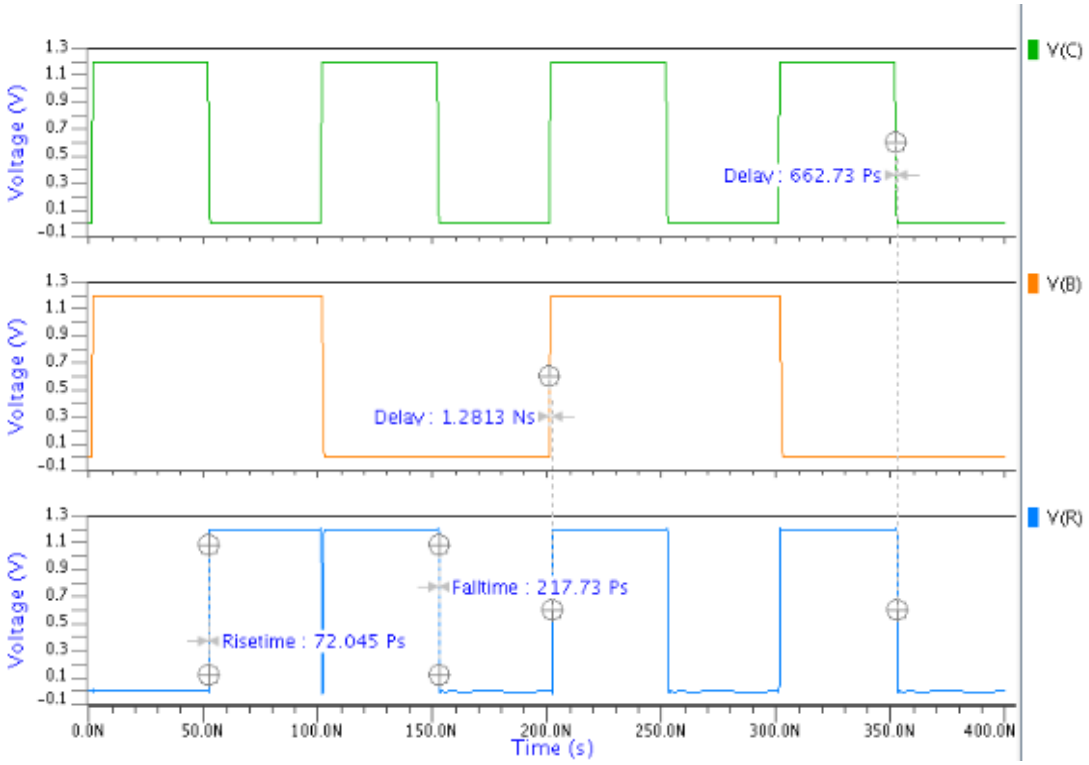

Figure 17. MTGDI Gate 5 Post Simulation Waveform (III)

7.Power Dissipation (µWatts) Analysis of MTGDI gates

To analysis the performance of the proposed full adder, it has been simulated for various voltages, ranges from 1.2V to 5V. The simulated value is presented in Table 4.12. For GDI and CMOS based design power dissipation is in terms of microwatts (µW) and other logic families such as TG, PT, CPL and DPL power dissipation is in terms of mille watts (mW). Although both GDI and CMOS dissipate power in microwatts range, GDI consume much less power compared to CMOS.

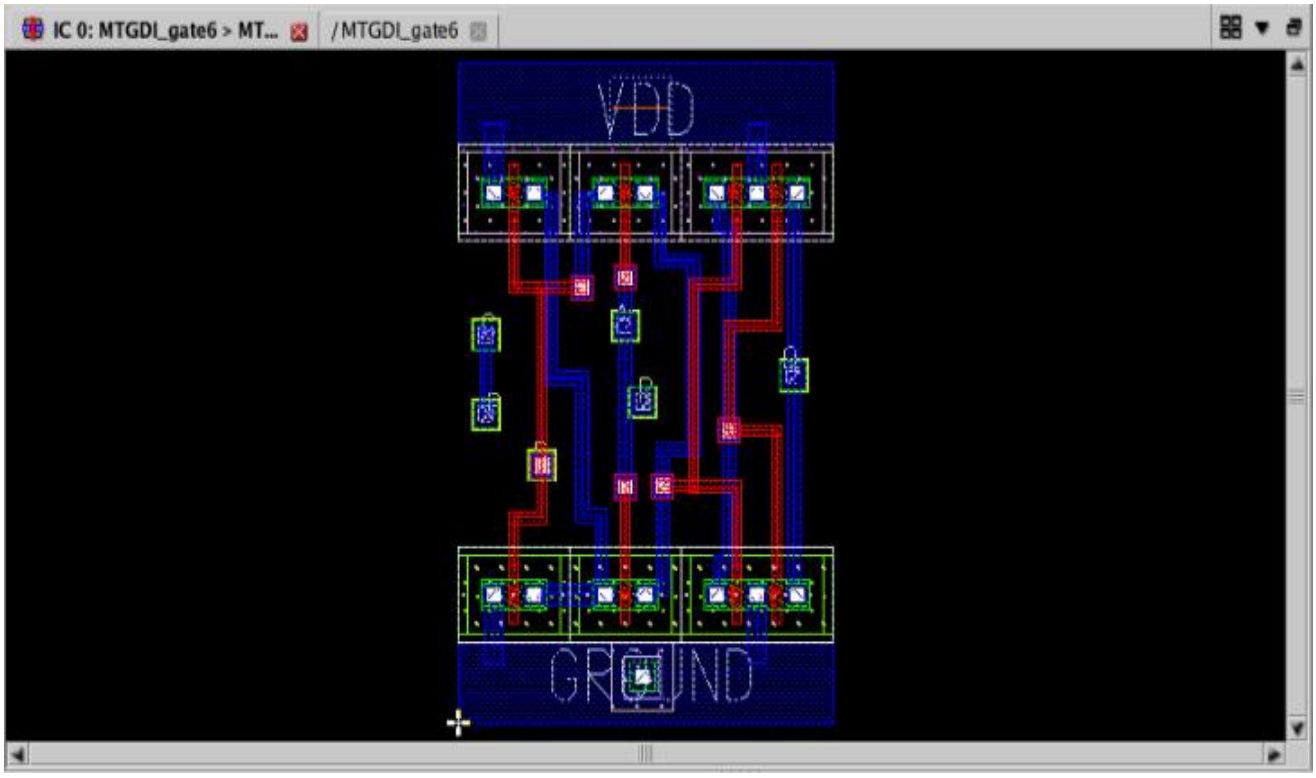

Figure 18. Layout of MTGDI Gate 6

8.Analysis of Simulated Results of 8-Bit Adder/Sub tractor

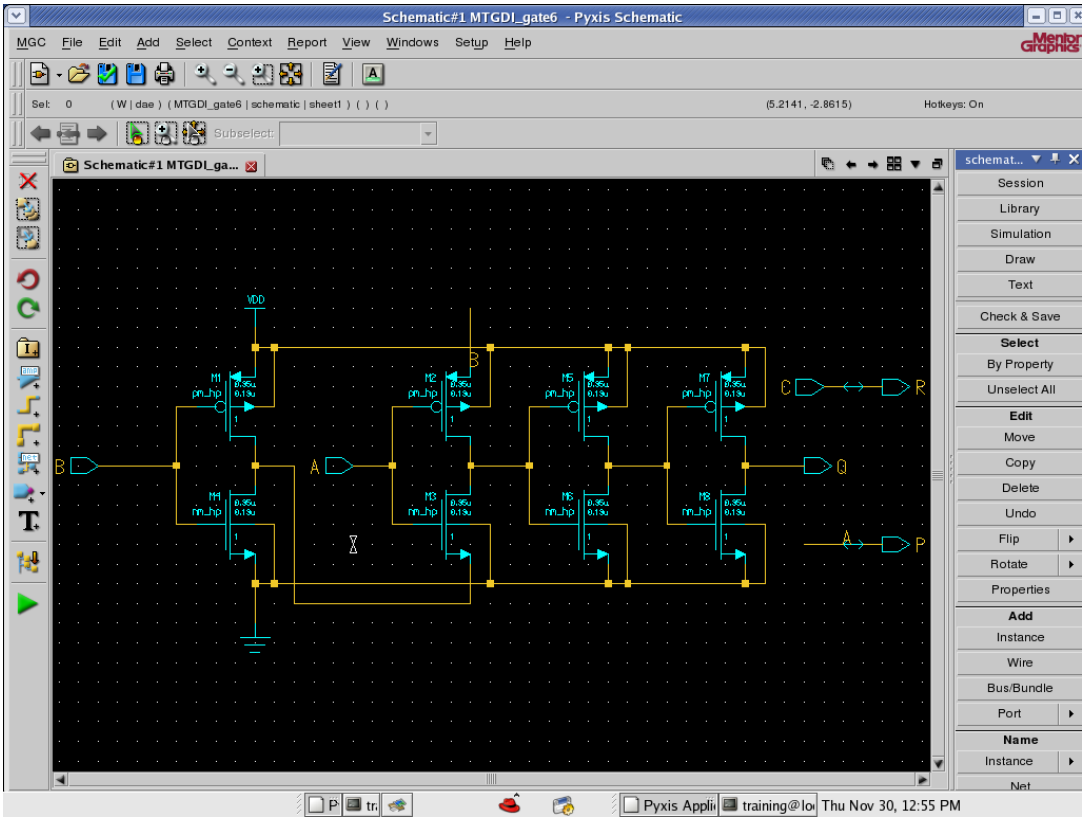

Figure 19. Schematic of MTGDI 6

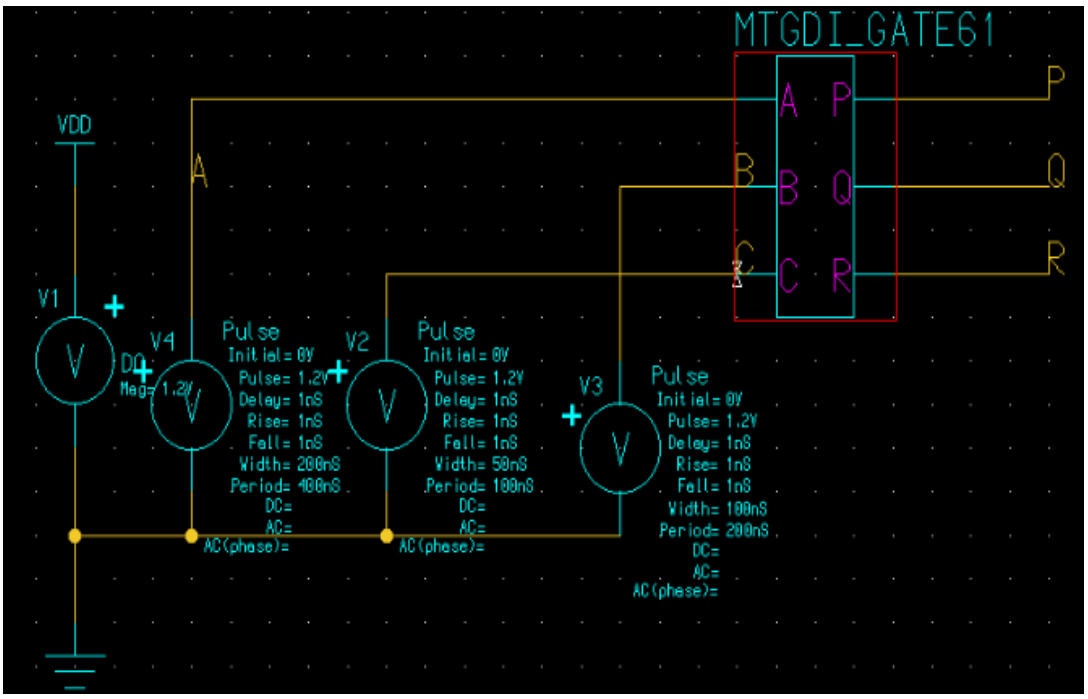

Figure 20. Simulation Mode of MTGDI 6

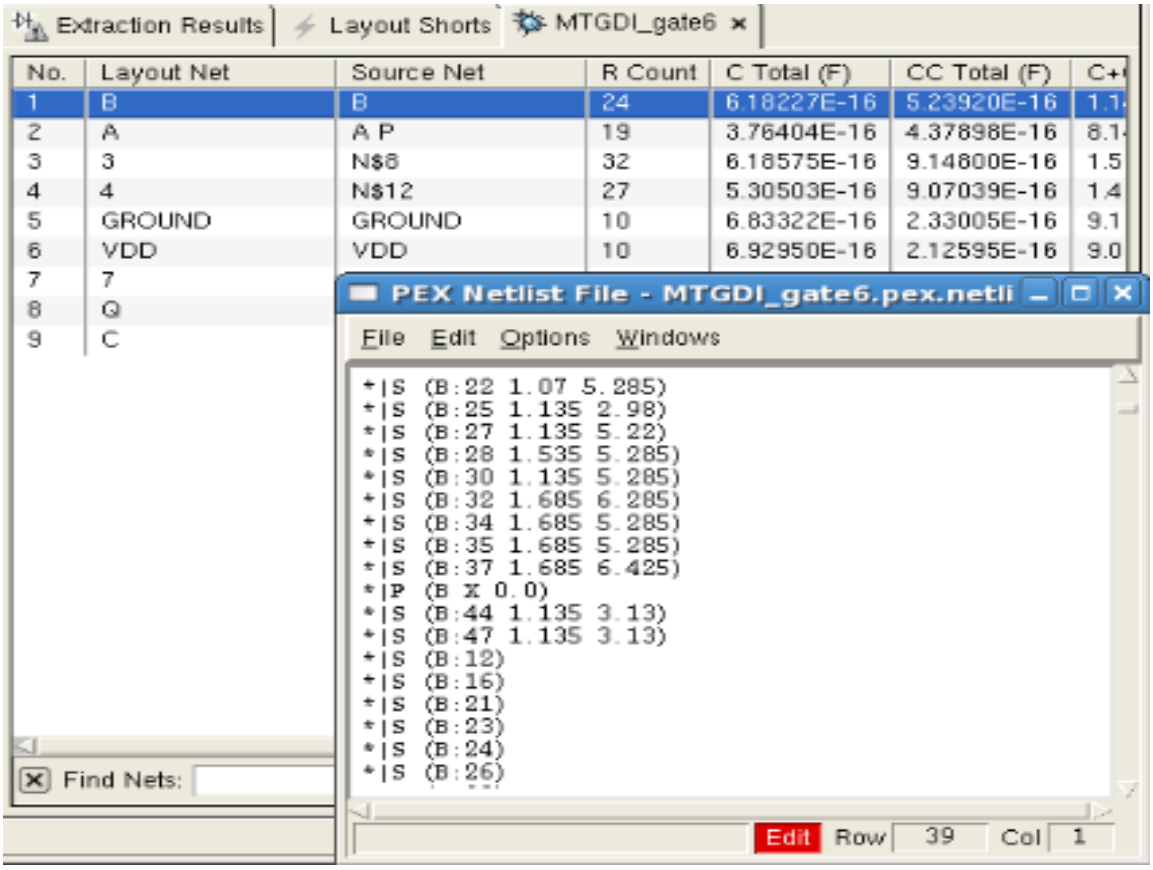

Figure 21. PEX for MTGDI Gate 6

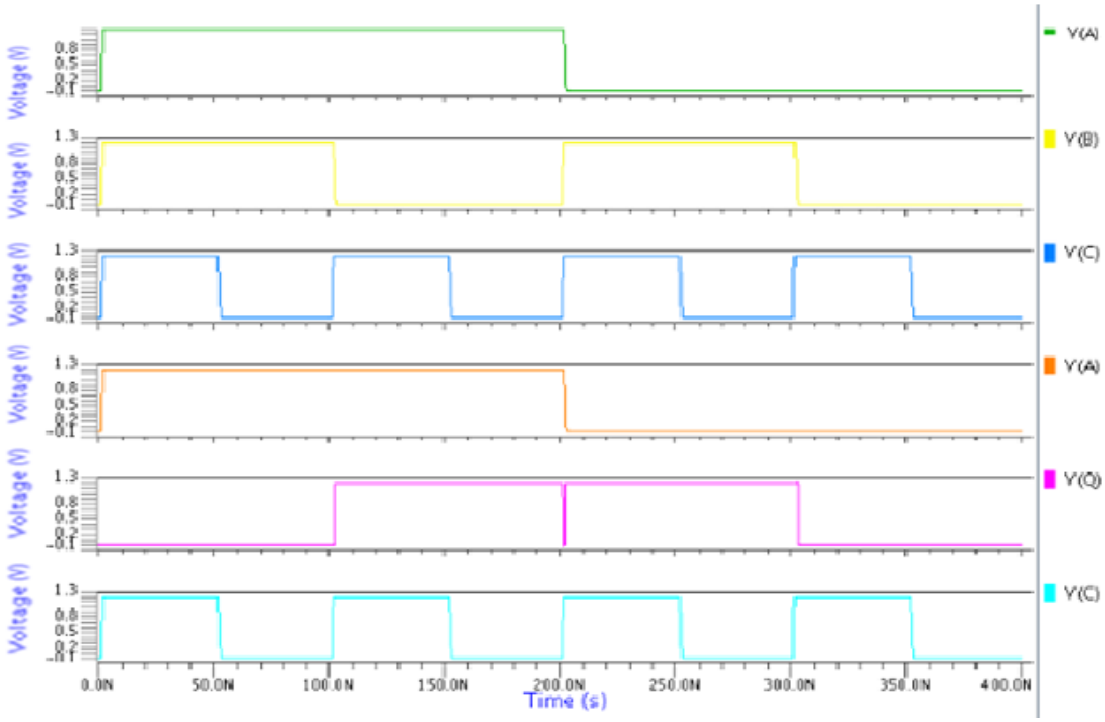

Figure 22. MTGDI Gate 6 Post Simulation Waveform (I)

9.Comparative Performance Analysis of Simulated Results of 8-Bit Adder/Su

Figure 13 shows the realization MTGDI gate3 which defines the functionality of two buffers and 2-input NOR or 2-OR depending on C input. The computation functions based on A, B, C are:

$$\text{If} \begin{cases} A=0, P=B, Q=0, R=XOR; A=1, P=B, Q=1, R=XOR \\ B=0, P=0, Q=A, R=XOR; B=1, P=1, Q=A, R=XOR \\ C=0, P=\overline{B}, Q=A, R=2-inputNOR; C=1, P=\overline{B}, Q=A, R=2-inputOR \end{cases}$$

5.

Table 4. Truth Table of MTGDI3 Gate

INPUT			OUTPUT		
A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	1	0
1	1	1	1	1	1

10.Comparative Performance Analysis of Simulated Results of 8-Bit Adder/Sub tractor

The functional description of adder/sub tractor module has been demonstrated in The proposed Adder/Sub tractor module is the derived structure designed from Ripple Carry Adder (RCA). The operation of both addition and subtraction can be performed by a common binary adder. This is done by including an Ex-OR gate with each full adder. Therefore, the RCA is modified selectively work in two operations: (i) not flip the bits and not add an extra 1 for the addition operation, or (2) flip the bits of the B operand and then add an extra 1 for the subtraction operation. The performance of proposed 8bit adder/sub tractor is presented in Table 4.

Conclusion

This paper focus mainly the effect of the design of the base reversible logic circuit in the overall design and proposed a low power reversible design with gate diffusion input technique. The proposed reversible logic was designed and simulated using mentor graphics software with Pyxis design manager. Gate diffusion input CMOS logic style used in this work provides low power design as Compared to other logic design techniques. It also presents an area efficient approach to low power, as GDI requires a smaller number of transistors as compared to other techniques, The implementation reversible logic cells (MTGDI) using Gate diffusion input technique has been presented. The functionality realization and performances are reported in chapter 4 and 5. Using the proposed MTGDI cells reversible full adder circuit has been implemented and its performance has been evaluated in terms of delay, power, PDP, garbage output, critical path and quantum cost. From the performance evaluation, it is observed that the proposed full adder using MTGDI is superior in terms of delay, PDP, power and quantum cost with respect to its counterpart. Nearly 20% of delay, 48% of power and minimum garbage and minimum cost are obtained for the proposed reversible full adder circuit using MTGDI gates. The simulation results of the reversible circuits implemented in GDI are very promising and have shown an intense potential to be the way to-go for the low power VLSI design.

Acknowledgement

For the future work, it is important to experience transistor exact behaviour in low voltage as we saw and discussed about some uncertainty and discrepancy in simulation in that region. The current architecture is very easy and uses easy and straight forward logics. The key parts perhaps are the starving mechanism which requires more investigation for better linearity. Current architecture uses two pulse generators for the carry and the sum circuits; however, it is possible to ratio the inverters and use only one pulse generator. This can reduce number of transistors almost 30%. Using other architectures to implement majority factor and doing more tests and comparison would be very suitable.

Table 5: Performance analysis of 8bit adder/Sub tractor module

Reversible Adder	REVERSIBLE GATE USED	DELAY SUM (ns)	DELAY COUT (ns)	Total delay (ns)	SUM		COUT		PWR (mW)	PDP mW × ns in fW-s	Garbage output	Critical path	Quantum cost
					RT (ns)	FT (ns)	RT (ns)	FT (ns)					
[9]	DKG	72.89	33.45	106.34	1.23	2.34	1.33	1.52	223.23	23738.278	8/cell	5	21
[11]	MKG	81.11	40.35	121.46	2.56	2.45	1.44	1.52	304.52	36986.999	6/cell	6	19
Proposed	3 MTGDI gate6 + 1 MTGDI gate1	63.45	28.92	92.37	1.34	1.23	1.31	1.23	189.45	17499.497	6/cell	4	17

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